APPLICATION NOTE

Improved Picture Quality Module MK8

AN98043

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Abstract

The Improved Picture Quality (IPQ) module MK8 is a application PC-board designed to evaluate the SAA 4977 and demonstrate its features.

The SAA 4977 is a video processing IC providing analog interfacing, video enhancing features, memory controlling and an embedded 80C51 µC core. It is especially applicable for 1•fH to 2•fH scan conversion using a 2M9 field memory.

Purchase of Philips I^2C components conveys a license under the Philips I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

APPLICATION NOTE

Improved Picture Quality Module MK8

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Summary

The SAA 4977 is a video processing IC providing analog interfacing, video enhancing features, memory controlling and an embedded 80C51 µC core. It is especially applicable for $1 \bullet f_H$ to $2 \bullet f_H$ scan conversion using a 2M9 field memory.

This application note gives an overview of the functions of the SAA 4977 and describes an application board designed to evaluate the IC and demonstrate its features. As many features depend on the program code implemented on the chip, the relevant software user guide is also necessary for operating the board.

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1. Introduction

The MK8 module is a 100 Hz scan converter based on the video processing IC SAA 4977. This IC makes possible a much simpler and cost-effective solution in designing a scan rate converter, compared to previous modules like MK7 or MK6. With A/D and D/A converters on chip 100 Hz display in an economical A-A-B-B mode is now possible using only one field memory and a display PLL circuit besides the SAA 4977.

This application note describes the hardware functions of the SAA 4977 and the application environment needed to realize 100 Hz scan conversion as well as extra functions. The internal software of the SAA 4977 defines the functions that are available to the user, so to actually run the module and invoke all features the user manual for the implemented software is also necessary. This manual is available as a separate document.[1]

The module MK8 is designed to be assembled with only one field memory besides the SAA 4977 for a low-cost solution, or with two field memories and the SAA 4990 for improved quality scan conversion and extra features.

2. Features of the MK8 module

The SAA 4977 itself has the following features and functions built in and therefore simplifies the design of a scan rate converter drastically:

- Internal prefilters
- Clamping
- Analog AGC
- Triple YUV 8-bit A/D converter
- 4 : 1 : 1 I/O interfaces
- Line locked acquisition PLL
- Horizontal compression
- Digital color transient improvement (DCTI)
- Luminance peaking
- Triple 10-bit D/A converter
- Memory controller
- Microprocessor with embedded ROM
- I^2C bus interface
- SNERT interface

With one field memory attached the module offers

- scan conversion from 50/60 Hz to 100/120 Hz in A-A-B-B mode (field repetition)
- still picture

If the board is equipped with the SAA 4990 and a second field memory the following features basically are possible (actual implementation depends on software, see appropriate user manual):

- scan conversion with line flicker reduction (LFR) in A-A*-B*-B mode
- progressive scan
- frame repetition mode for movie sources
- advanced still picture (A-A*-A-A*)
- noise reduction

1. Lahann, Nils: I^2C-bus register specification for BESIC, Philips Semiconductors User Manual UM9701

3. Functional description of the SAA 4977

The SAA 4977 provides the interfaces for digital video processing in an analog environment, it generates the control signals to run the field memory, it has on board a microprocessor with embedded ROM, and also offers various processing functions on the video data. For performance reasons the IC consists of two chips (multi-chip module), the first one (acquisition chip) providing mostly analog functions and the second one (display chip) mainly digital functions and controlling. Fig. 1 shows the block diagram of the SAA 4977.

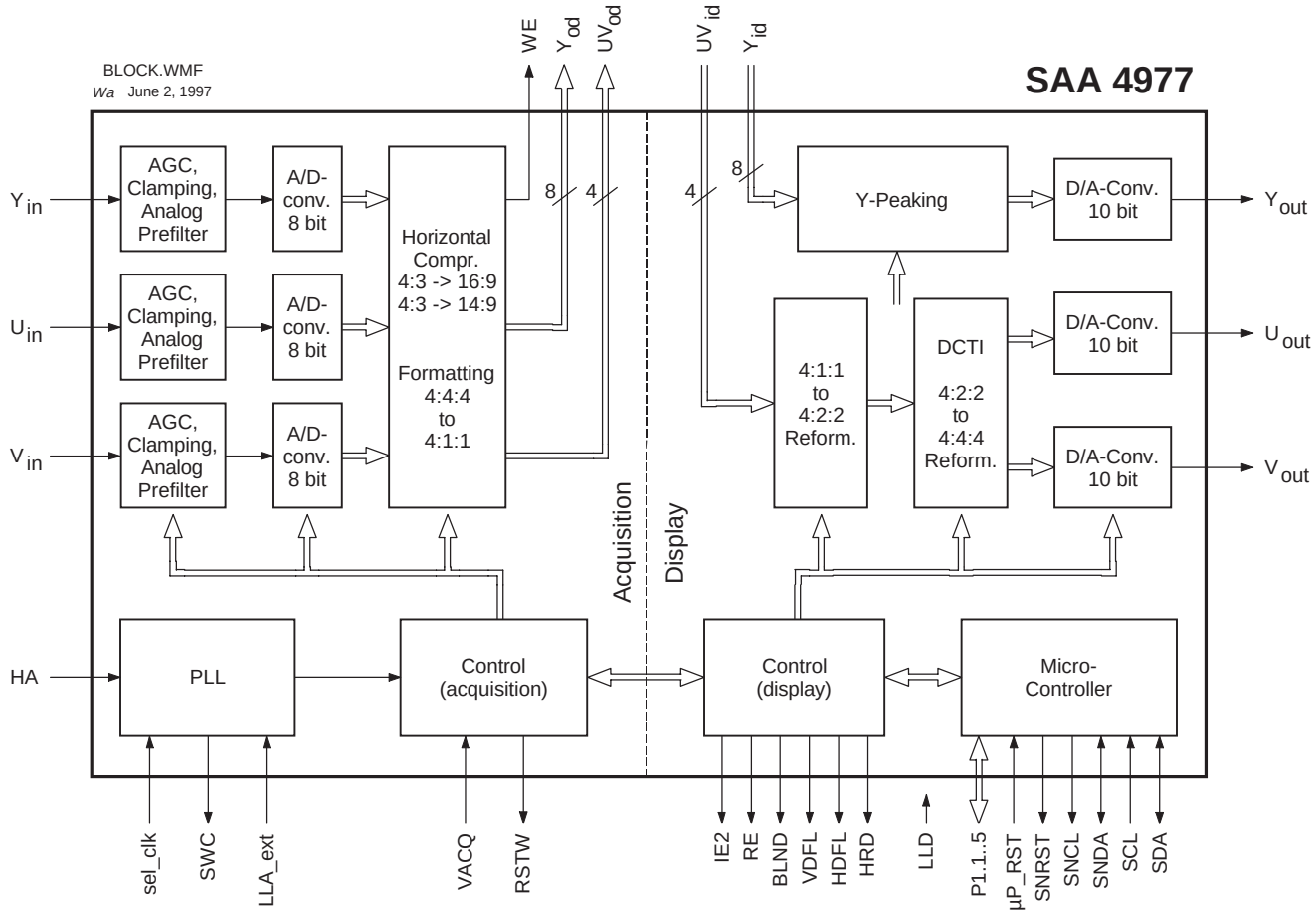

Fig. 1 Block diagram of the SAA 4977

3.1 Analog input processing

At the input of the acquisition chip each of the analog input signals Y, U and V is gain controlled, clamped and low pass filtered, before it is converted to the digital domain by three 8-bit A/D converters.

The gain control unit permits an amplification of -3 dB to +6 dB in steps of 0.4%, a step size hardly visible. Luminance and chrominance gain settings can be controlled separately. The settings are under control of the microcontroller which is therefore needed to set up an automatic gain control loop.

Each input channel has its clamping circuit. For luminance the black level is set to digital level 16, for U and V the colorless level is set to the center level of the A/D converters. The clamping pulse is generated internally.

Before the signals are A/D converted they pass an analog low pass prefilter. The bandwidth of this filter is -3 dB at 6 MHz, a notch is provided at f_{dk} (16 MHz). For the prefilter a bypass can be activated.

Three A/D converters are used to convert Y, U and V into digital data. They are identical, are 8 bit wide and run at 16 MHz data rate.

At the output of the A/D converters an overflow detection is provided. The threshold for this overflow can be selected by software between 216, 224, 232 and 240. The overflow occurrences are summed up in a register the highest 8 bits of which can be read by the microprocessor. In this way an automatic gain control loop can be established.

3.2 Digital processing at $1f_H$ level

Some digital data processing is done at the $1f_H$ level (16 MHz) in the acquisition chip, before data is written to the field memory.

Since all three A/D converters run at 16 MHz, this data format of 4:4:4 needs to be reduced to 4:1:1 to fit into the memory. This conversion is done in two steps. The U and V data are low pass filtered and then down sampled by a factor of two, low pass filtered again and down sampled a second time by a factor of two. Finally the data is formatted into the 4:1:1 format, see fig. 2. In this format the chrominance information is distributed over 4 clock periods, the first data word beginning one clock period after the rising edge of the WE signal.

For displaying a 4:3 sources on a 16:9 screen a horizontal signal compression can be activated. The compression factor in this case is 4/3 = 1.33 (16:9 mode). For a slighter compression mode also 7/6 = 1.16 is selectable (14:9 mode).

When compression is active, a reduced number of pixel data per line is generated. To achieve this at the same clock frequency every 4th (in 16:9 mode) or every 7th (in 14:9 mode) pixel is discarded (memory writing disabled). The remaining ones are derived from an interpolation unit where a variable phase delay filter is used. This filter ensures a high accuracy in interpolation.

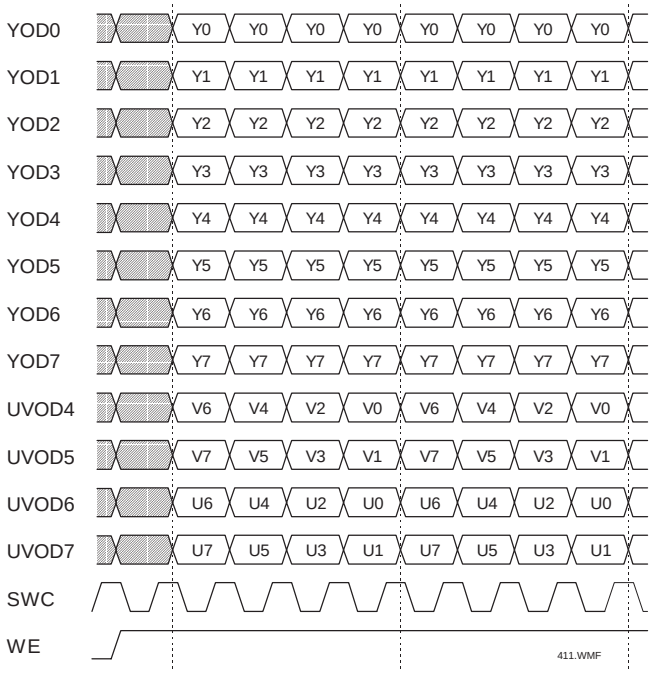

Fig. 2 4:1:1 data format

3.3 Digital processing at $2f_H$ level

From the acquisition chip the digital video data is written to a field memory. Reading is done at twice the clock rate by the display chip of the SAA 4977.

3.3.1 Signal data range

Signal data on the display chip are processed using a 10 bit wide data range. The user can select how this extended range is to be used. With *output range = 1* the full 10 bit range is used for the nominal signal. The black level is now at 64 and has the same relative level compared to the 8 bit input signal. With *output range = 0* basically a 9 bit range is used for the nominal signal. The black level is at 288 and the white level at 767. This leaves ample room for signal over- and undershoots. The relations are depicted in fig. 3.

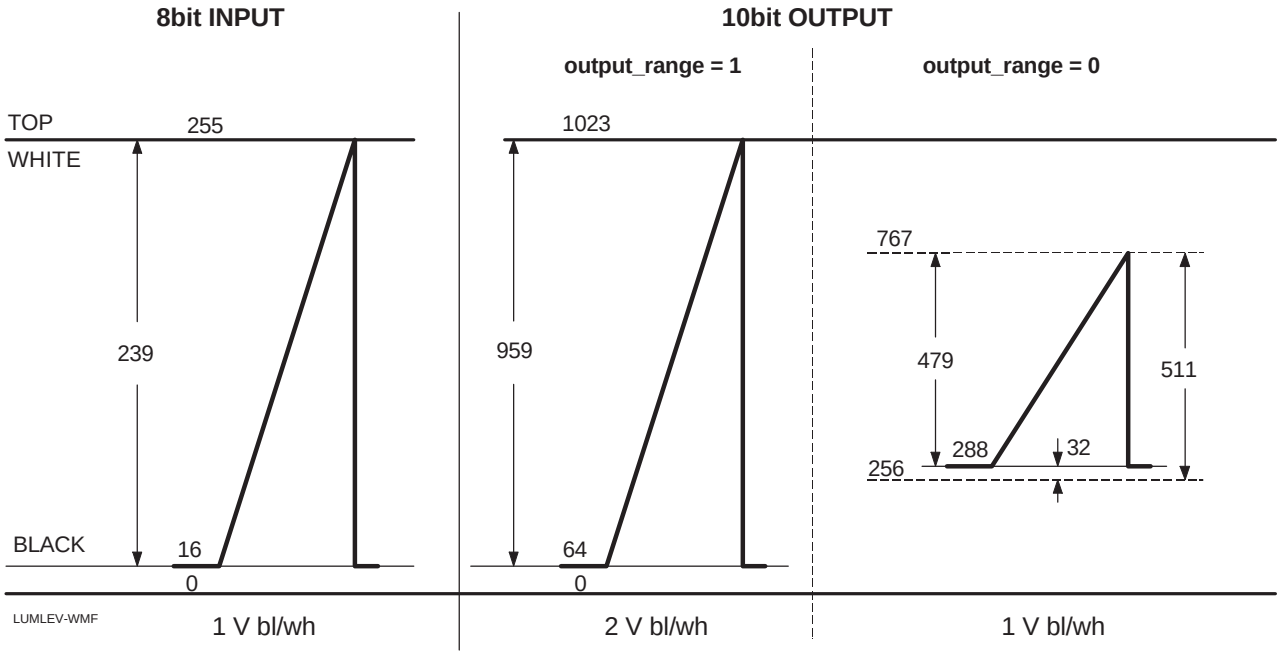

Fig. 3 Output signal levels

3.3.2 Luminance Peaking

The luminance signal Y is processed by the peaking circuit of the display chip in order to boost the higher frequency ranges. A block diagram of the circuit is shown in fig. 4. The circuit uses a combination of two band pass filters and a high pass filter having their maximum gain at $f/f_c = 0.15$, $f/f_c = 0.25$ and $f/f_c = 0.5$ resp., the output of which is added to the original signal. The influence of each of the filters can be adjusted in eight steps from 0 to 8/16 (7/16 omitted). In fig. 5 to 7 the frequency response of each filter is given for different values of *tau* (band pass 1), *alpha* (band pass 2) and *beta* (high pass). Fig. 8 gives an example of two transfer curves having different center frequencies.

The peaking filter will boost higher frequency signals regardless of their amplitude. For structured small signals this will lead to unwanted coring. In order to prevent this the block *wide coring* is added. It suppresses any gain for low amplitudes, so the original luminance signal is not influenced. The coring threshold level can be set by the parameter *corthr*. This 4 bit parameter allows 16 settings from 0 ... 120 in steps of 8. The value of 0 ... 120 has to be seen in relation to a signal amplitude ±1023, so the maximum setting equals roughly one eighth of the signal amplitude. The transfer curve is depicted in fig. 9.

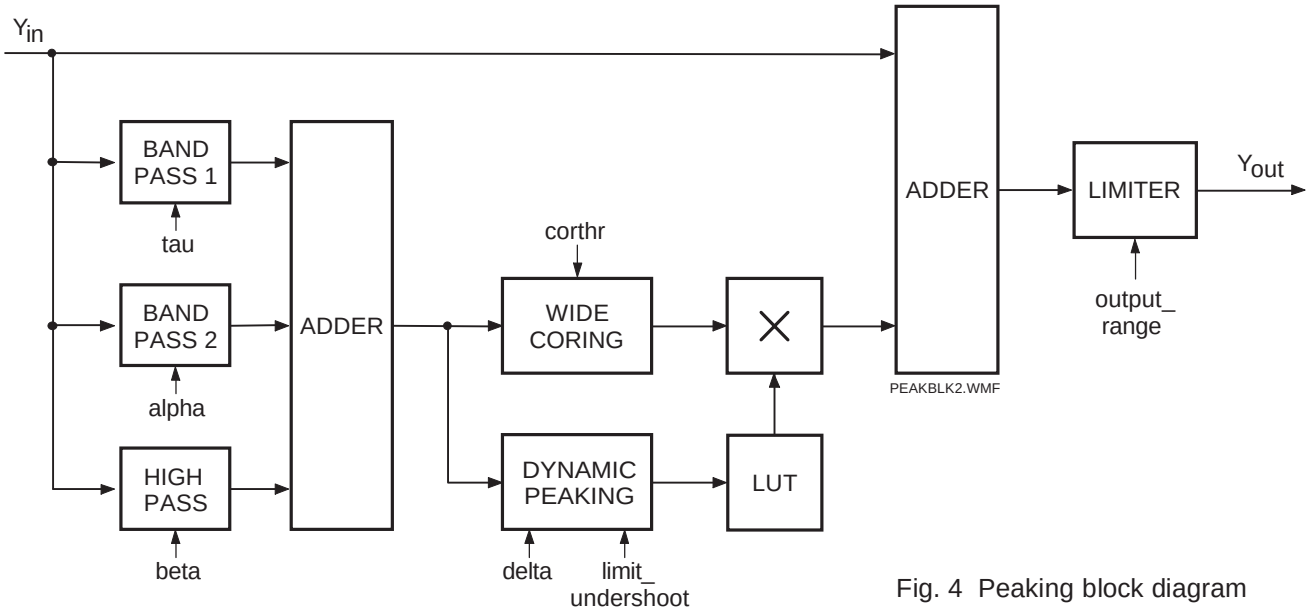

Fig. 4 Peaking block diagram

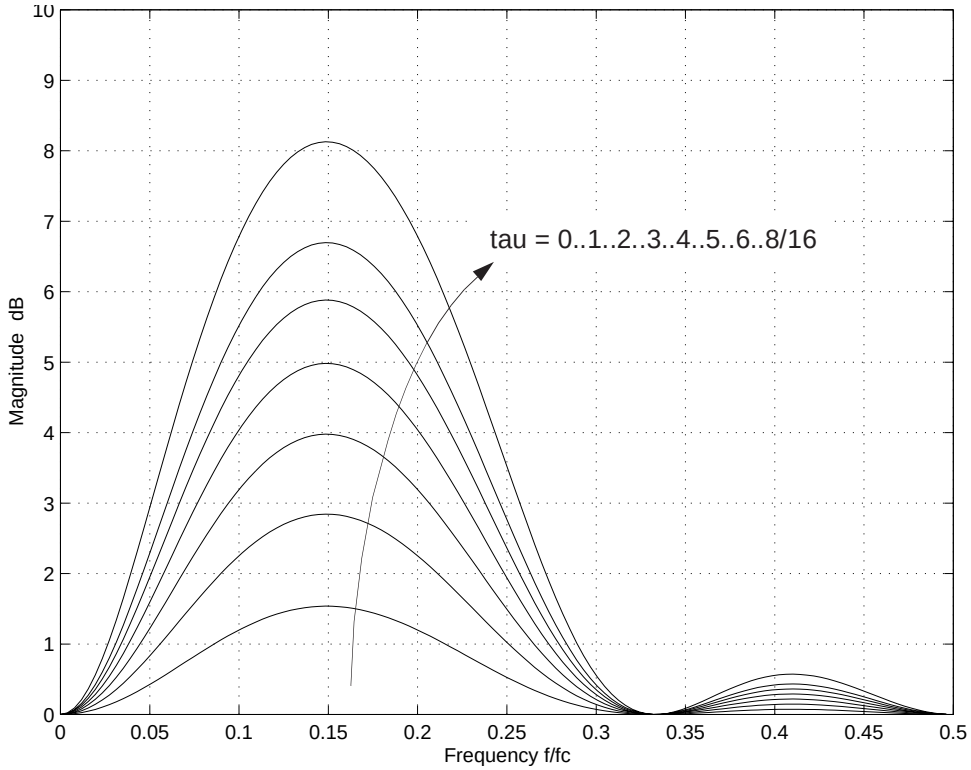

Fig. 5
Frequency response of the peaking band pass filter 1

More influence on the peaking function is possible in the block *dynamic peaking*. By changing the parameter delta the gain of the peaking function can be made dependent on the amplitude. For *delta = 0* the gain is constant for all amplitudes, while with *delta* increasing up to 3 gain is more and more reduced for high amplitudes.

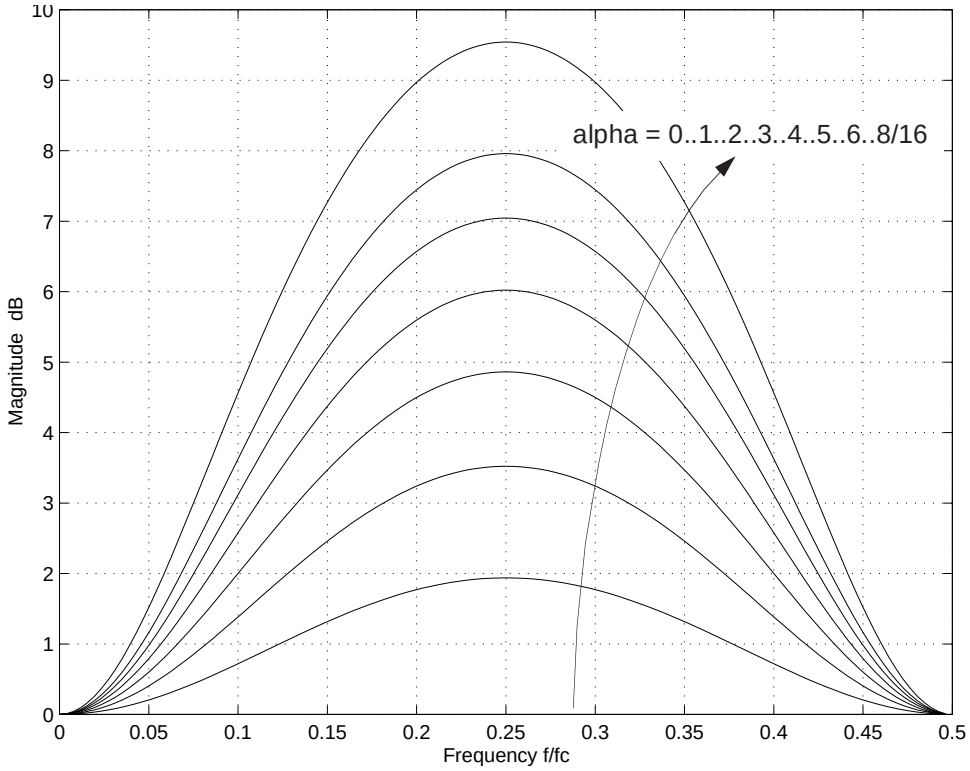

Fig. 6
Frequency response of the peaking band pass filter 2

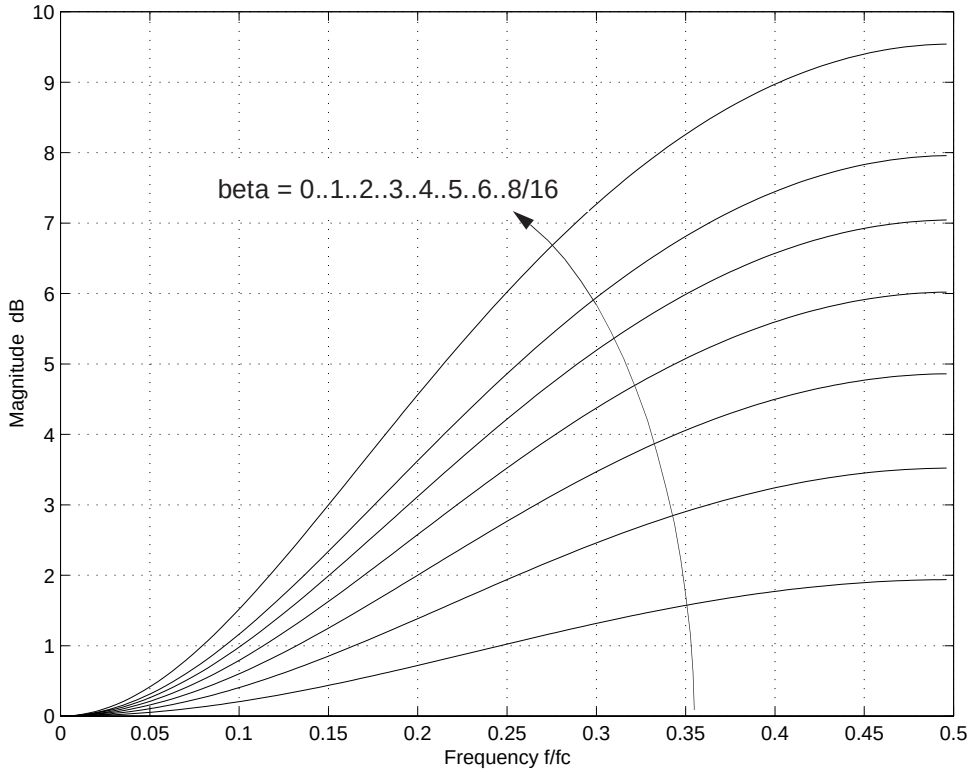

Fig. 7
Frequency response of the peaking high pass filter

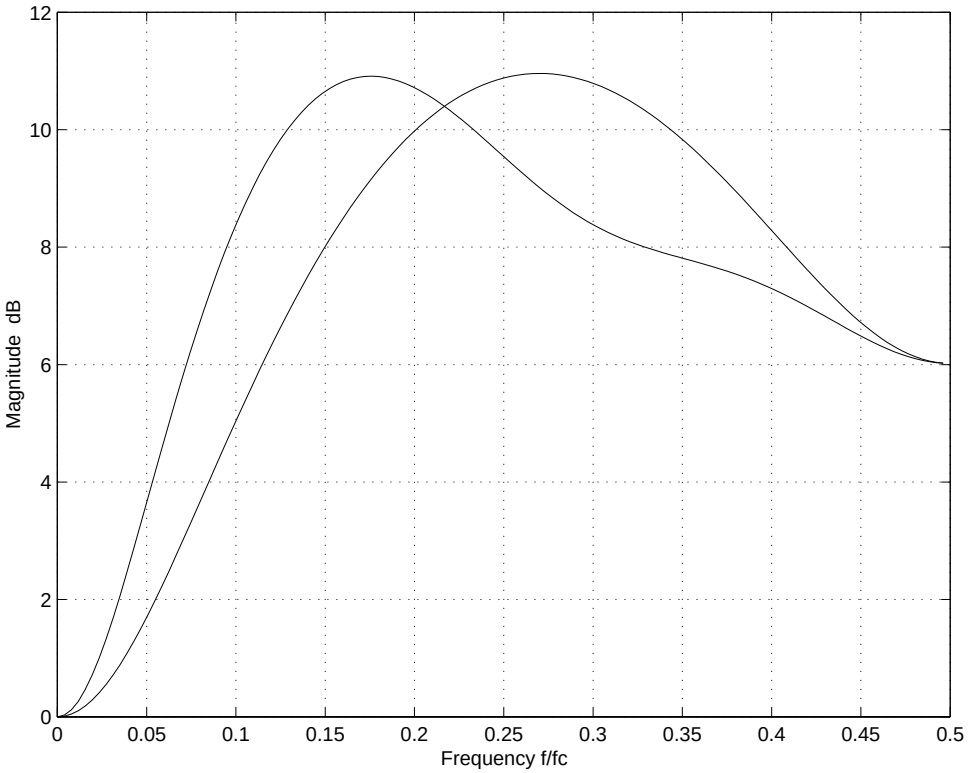

Fig. 8
Variation of peaking center frequency

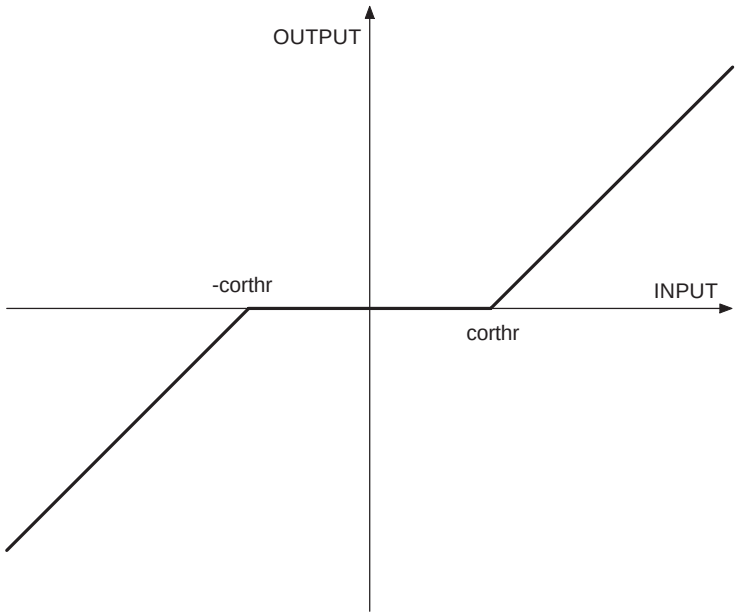

Fig. 9 Luminance coring

By changing the parameter *limit_undershoot* the peaking function can be reduced for negative going signal transients. This is to prevent signal undershoots from going below the black level. *Limit_undershoot* is a 2 bit parameter. Limiting is off for a setting of 0 and maximum for a setting of 3.

3.3.3 Digital color transient improvement (DCTI)

U and V data are reformatted from 4:1:1 to 4:2:2 using a linear interpolating filter. Further upsampling to the 4:4:4 format occurs during the DCTI process.

The Digital Color Transient Improvement (DCTI) is intended for U and V signals originating from a 4:1:1 source. Horizontal transients are detected and enhanced without generating overshoots.

The data path delay is varied on the basis of a function of the second derivative of the U and V signal. The effect at an edge is that during the first half the data path delay is higher than nominal and in the second half it is lower than nominal. This will make the edge much steeper. As this interpolation is done with the resolution equal to that of the Y samples a 2:1 interpolation is performed generating a 4 :4 :4 format for the D/A converters.

The DCTI function can be controlled mainly by adjusting the parameters *gain* and *limit*. *Gain* influences the resulting steepness of the output signal, whereas *limit* affects the maximum amount of data path delay. Modifications of these parameters are depicted in the fig. 10 and fig. 11 using a maximum amplitude color transient as input signal. Both *gain* and *limit* must be greater than zero for DCTI to be active.

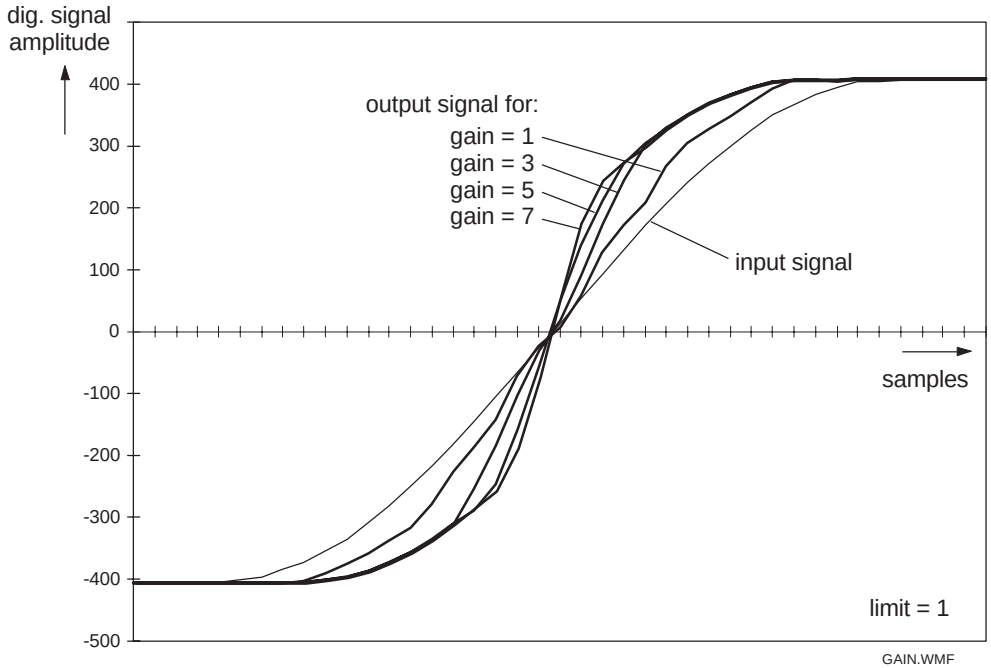

Fig. 10 DCTI with variation of gain for a limit setting of 1

An artefact of this processing becomes apparent when two edges are close together in the video. During the second half of the first edge a delay is chosen that will collect video data from where the second edge is already active. The same is valid for the second edge. The result of this processing on a video pulse, which is looking like a hill, is that of a hill with one or two bumps on it. To prevent this from happening, the positions where the first derivatives in U and V change sign, are marked and used to limit the range of the relative delay. This function is called ‘over the hill protection’. It can be turned on and off. Figures 12 and 13 show the effect of the DCTI function with and without ‘over the hill protection’ when applied to a hill-shaped video pulse.

The ‘hill protection‘ function still produces artefacts for signal transitions where the first derivative does not change sign, i. e. two (or more) positive (or negative) steps following each other. Signals of this kind are handled properly if ‘superhill protection‘ is turned on. The behaviour of DCTI with active and inactive ‘superhill protection‘ is shown in fig. 14 and 15.

The DCTI function can be controlled by the parameter *separate* in regard to whether both signals U and V are processed together or each one separately. In case of *separate* = 0 (off) a steep transition in either signal is suf-

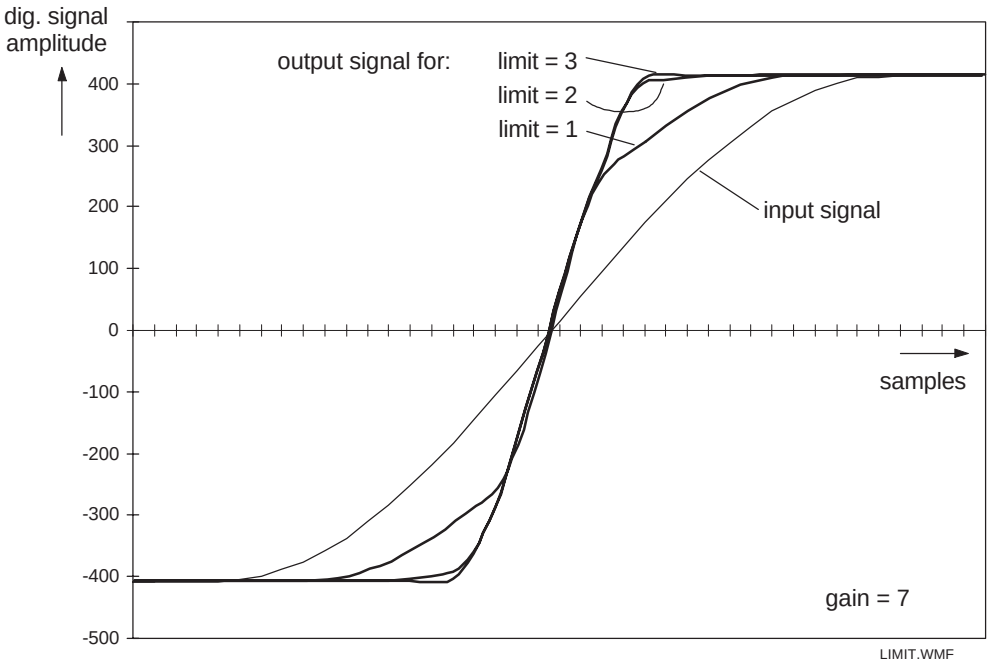

Fig. 11 DCTI with variation of limit for a gain setting of 7

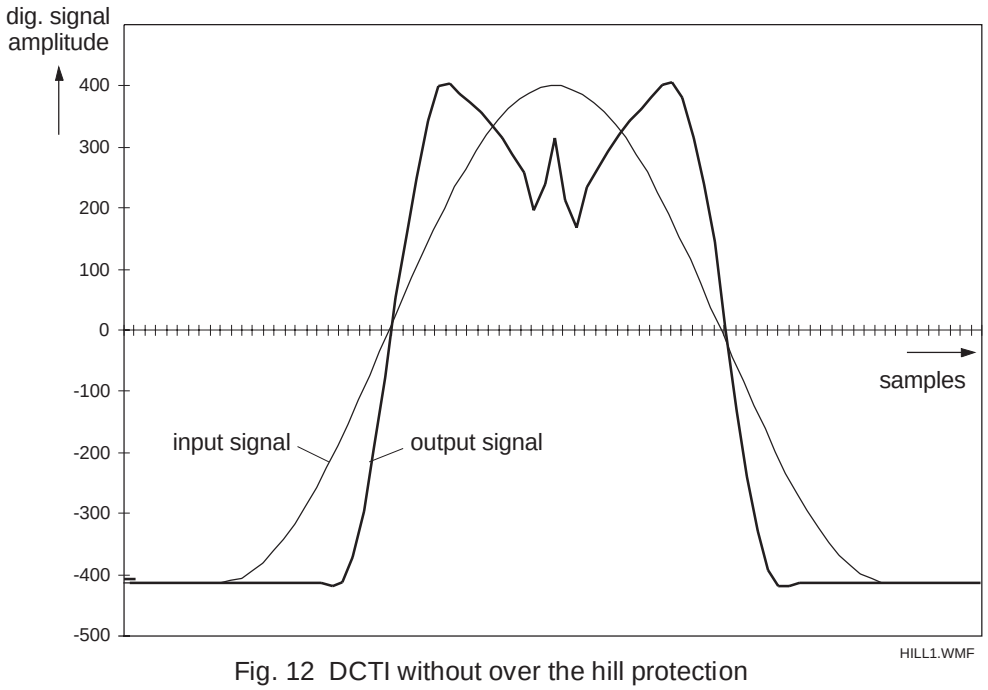

Fig. 12 DCTI without over the hill protection

ficient to activate the data path delay variation. This setting is based on the fact that most color transients involve both signals U and V. And if one of the signals stays constant, a data path variation would do no harm.

In case of *separate* = 1 (on) each signal is processed separately. This setting is favorable if the transitions in both signals do not occur at the same time. Common processing then would give false colors which can be annoying. An example for processing such signals is given in fig. 14 and 15.

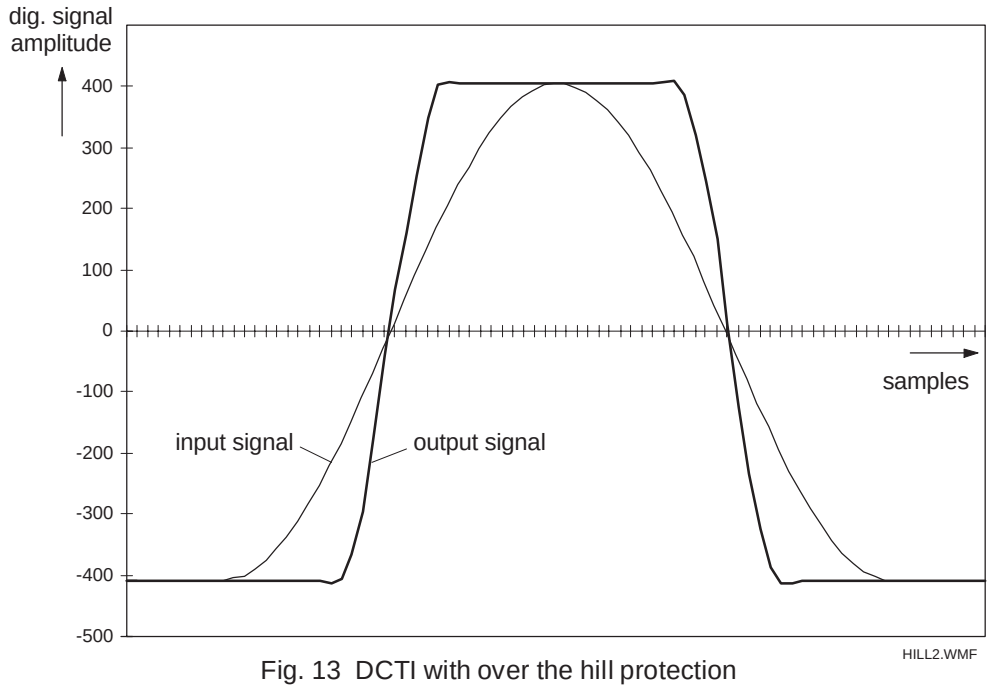

Fig. 13 DCTI with over the hill protection

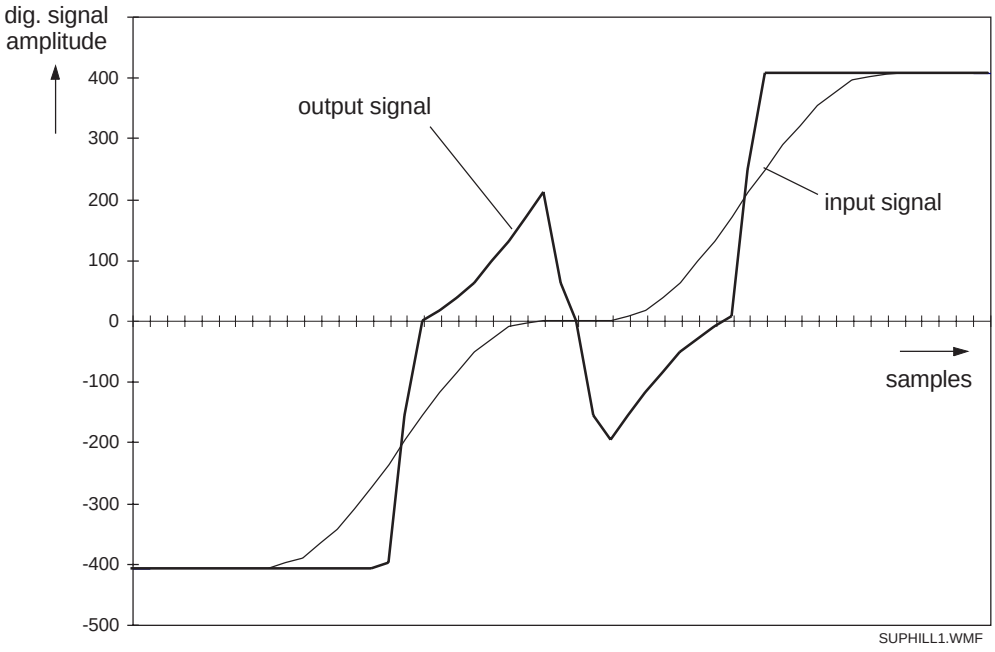

Fig. 14 DCTI with superhill-protection off

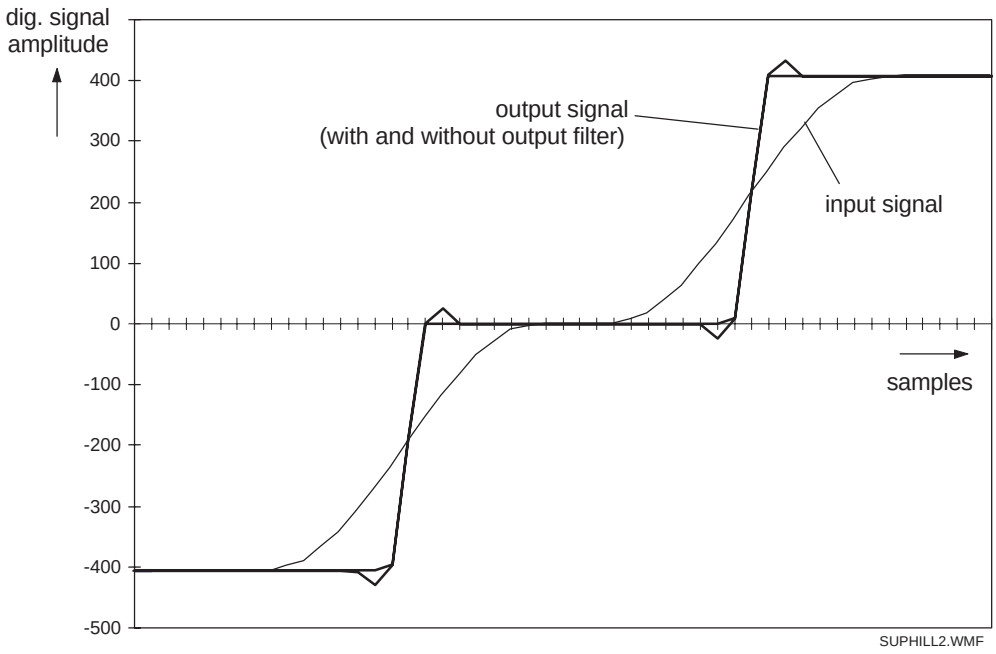

Fig. 15 DCTI with superhill-protection on

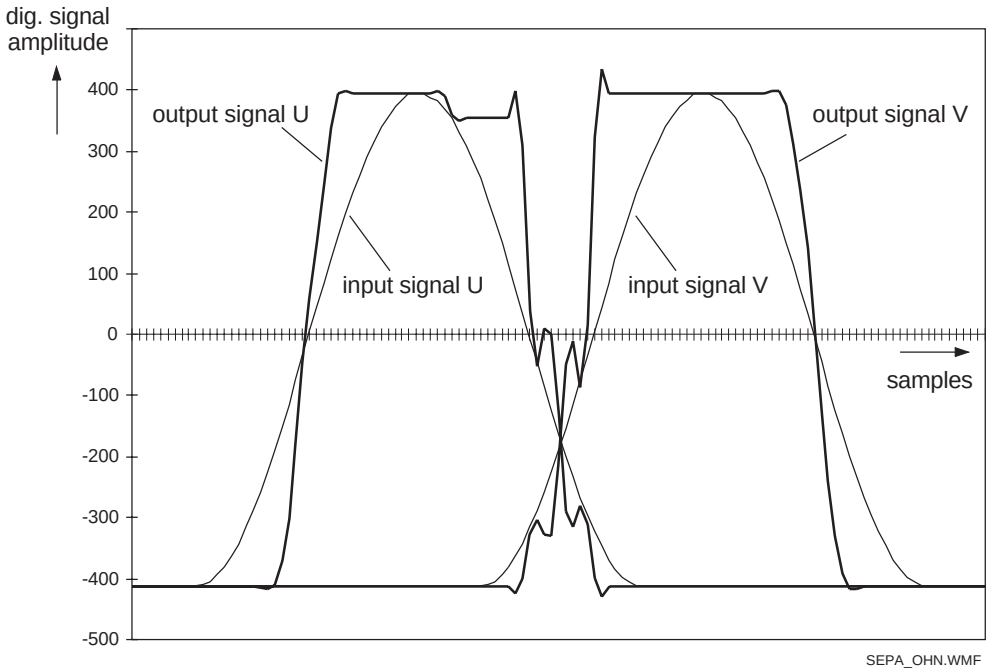

Fig. 16 DCTI with common processing of both signals (*separate* = 0)

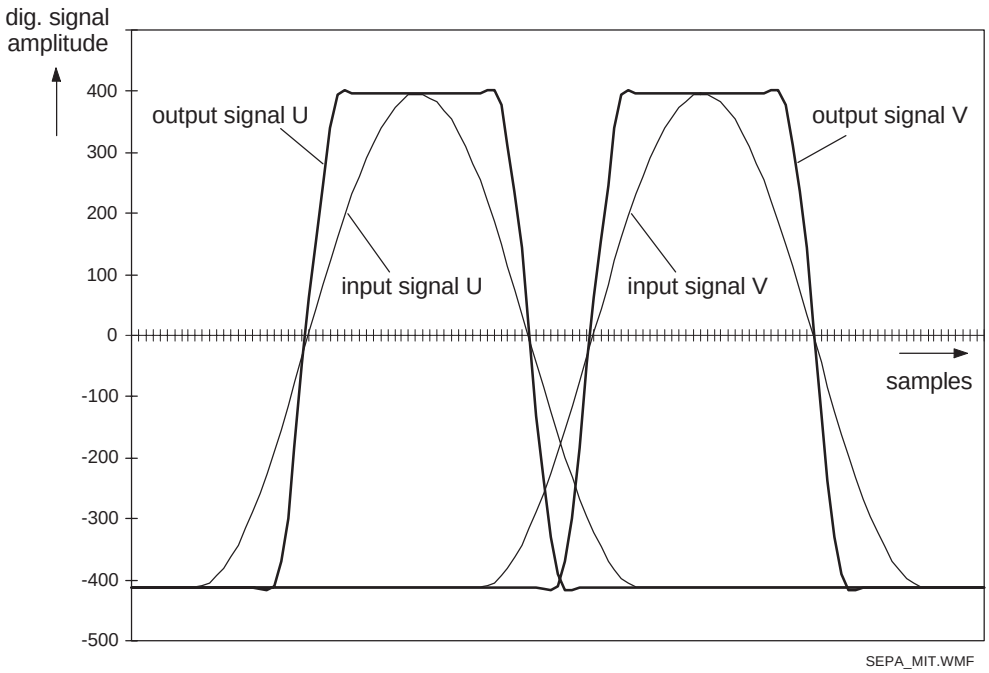

Fig. 17 DCTI with separate processing of both signals (separate = 1)

4. Controlling

4.1 Acquisition PLL

The acquisition chip of the SAA 4977 contains the acquisition PLL. The rising edges of the external HA signal (horizontal acquisition pulse or H_{sync}) and the internally generated H_{ref} are compared, and the measured phase difference controls a clock generator. This clock generator runs at 32 MHz with a simple clock divider being used to generate 16 MHz. This ensures a perfect 50% duty cycle for the system clock LLA[2] of the acquisition chip.

A video line of 64 µs contains 1024 clock cycles of 16 MHz. Therefore the clock frequency is divided by 1024 to get the horizontal reference signal H_{ref}.

The acquisition system clock LLA can either be generated by the PLL or provided externally. In the latter case also a synchronous H_{ref} signal must be provided by the external application at pin HA. The external clock mode can be activated by pulling pin SEL_CLK to LOW. In external clock mode the internal PLL is switched off.

4.2 Memory controller

The on-chip memory controller provides the necessary control signals for one- or two-field memory concepts. The write signals for the first memory are derived from the acquisition clock, signals for reading are derived from the display clock. In order to achieve this the memory controller is divided into an acquisition part and a display part, with each part placed on the resp. chip. An asynchronous serial link provides communication between the two parts.

4.3 Microprocessor

The SAA 4977 contains an embedded 8051 microprocessor core including 256 Byte RAM and 16 kB ROM (µC). The microprocessor is placed on the display chip and runs on a 16 MHz clock, generated by dividing the 32 MHz display clock by a factor of 2.

A parallel port (PORT 1) can be used for application specific signals. While pins P1.0, P1.6 and P1.7 are already used for SNRST and the I^2C bus signals SCL and SDA resp., the port pins P1.1 ... P1.5 are still available for specific purposes.

Internally the microprocessor and the display part of the memory controller are connected by a parallel address and data bus. Via this bus the µC communicates with all parts of the chip. The memory controller serves as a router, distributing all display related write and read controls on the display chip and sending/receiving all acquisition related data via the serial link to/from the acquisition chip.

For communication with external ICs two serial busses can be used, the I^2C bus and the SNERT bus. The I^2C-bus interface is used in a slave receive and transmit mode for general communication with a central master microcontroller. Both standardized baud rates of 100 kBit/s and 400 kBit/s are supported.

The SNERT[3] bus is used for communication with slave ICs that also have this interface. It is a single master bus and uses the µC´s serial interface for transmitting and receiving data. Clock is supplied by pin SNCL while data is written or read through pin SNDA. These pins refer to the pins TxD and RxD of a standard 8051 µC, and the transfer mode is known as mode 0 of the serial interface. Address and data bytes are transmitted alternately. As reset signal the bus uses a third signal line (SNRST) to determine the correct address / data sequence as well as to update any readable registers in the devices. In a video environment however the vertical sync pulse is usually taken for this reset purpose, since SNERT transmissions are initiated by this pulse, too.[4]

2. LLA ... *Line Locked Acquisition* (clock)
3. SNERT stands for *Synchronous No-parity Eight bit Reception and Transmission*
4. see also: Waterholter, Heinrich: The SNERT bus specification, Philips Semiconductors Application Note AN 95127

5. MK8 Application Board

The SAA 4977 provides the interfaces between the internal digital processing and the analog environment. Luminance and color difference signals from a color decoder or other analog source can be directly input without any external filters. 10 bit D/A converters at the output provide the interface to an RGB processing circuit.

While the internal functions along the data path are always available, special 100 Hz features depend on external digital components. The simplest form of scan rate conversion is field repetition (A-A-B-B mode), this is possible with just one field memory of the SAA 4955 type connected. A block diagram of this configuration is shown in fig. 10.

An alternative of the SAA 4955 is the compatible SAA 4956. It is the same memory, but with a built-in field-based noise reduction circuit. The noise reduction function can be controlled by I^2C-bus. At the time this report is written the SAA 4956 is still in development.

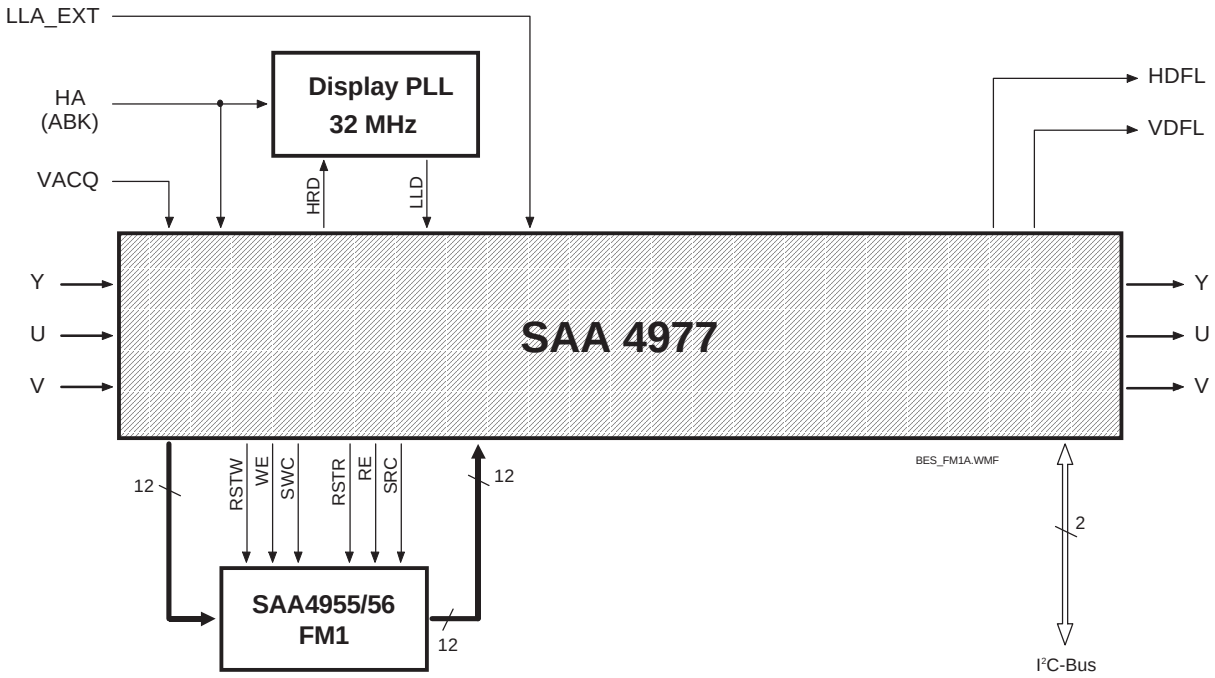

Fig. 18 Application block diagram of the SAA 4977 using one field memory

Additional functions like line flicker reduction (LFR), progressive scan, zoom and noise reduction are available if the IC SAA 4990 as well as a second field memory SAA 4955 is added. A block diagram of this configuration is shown in fig. 11.

Many functions are realized by software, so for an exact overview of what modes and features are available to the user refer to the appropriate software user manual.

An application board has been prepared to show the functions of the SAA 4977. It supports all configurations described above. The complete circuit diagrams are given in fig. 12 to fig. 16. 0-Ohm resistors are used to close the data path in case of the 1-field-memory concept, when no SAA 4990 is present, and also provisions are made on the board to use the SAA 4956 instead of the SAA 4955.

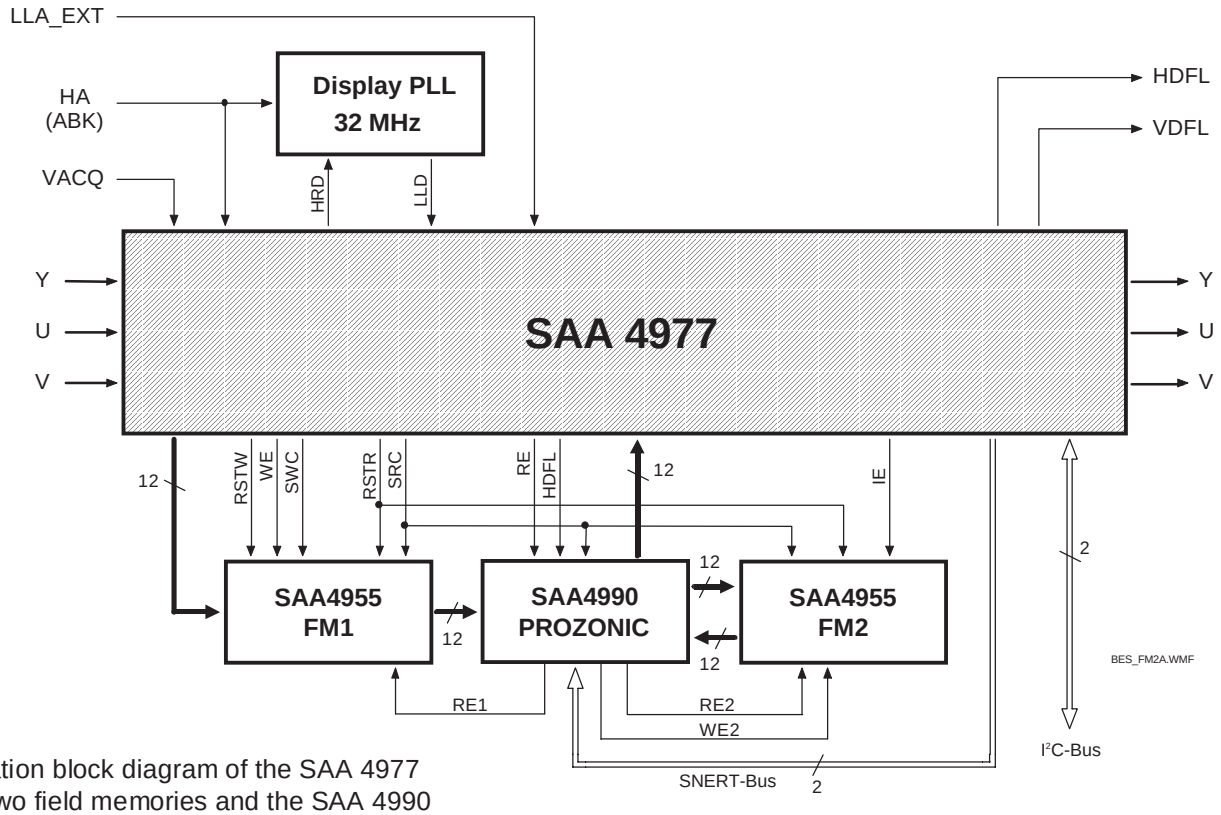

Fig. 19
Application block diagram of the SAA 4977 using two field memories and the SAA 4990

The SAA 4977 has several power pins for analog and digital supply both at 5V as well 3.3V, see table 1. As can

Table 1: Analog and digital supply pins

Analog supply		Digital supply	
+3.3 VA	**+5 VA**	**+3.3 VD**	**+5 VD**
pin 75: VDDA4	pin 23: VDDA1	pin 8: VDDD5	pin 18: VDDD1
pin 80: VDDA5	pin 25: VDDA2	pin 11: VDDD4	pin 19: VDDD0
	pin 29: VDDA3	pin 69: VDDD3	pin 46: VDDD2
			pin 67: VDDIO

be seen on sheet 5 of the circuit diagram (fig. 16), each positive supply has its own decoupling circuitry. Decoupling capacitors are spread across a large value range, so a wide-band suppression of supply noise is ensured. The positive supply voltages are fed through an inner layer of the 4-layer board, the other inner layer is completely reserved for ground. These two layers are closely on top of each other and thus further improve supply stability.

Special care is taken to supply the PLL circuit. Its voltage of +5VP has its own stabilizer. +8VA is used for the analog output amplifiers and filters.

For testing and measurements of the SAA 4977 several power supply lines are equipped with test pins, and provisions are made to break up the on-board supply for external feeding. Input and output signals as well as a few other signals are also provided with test pins for easy monitoring.

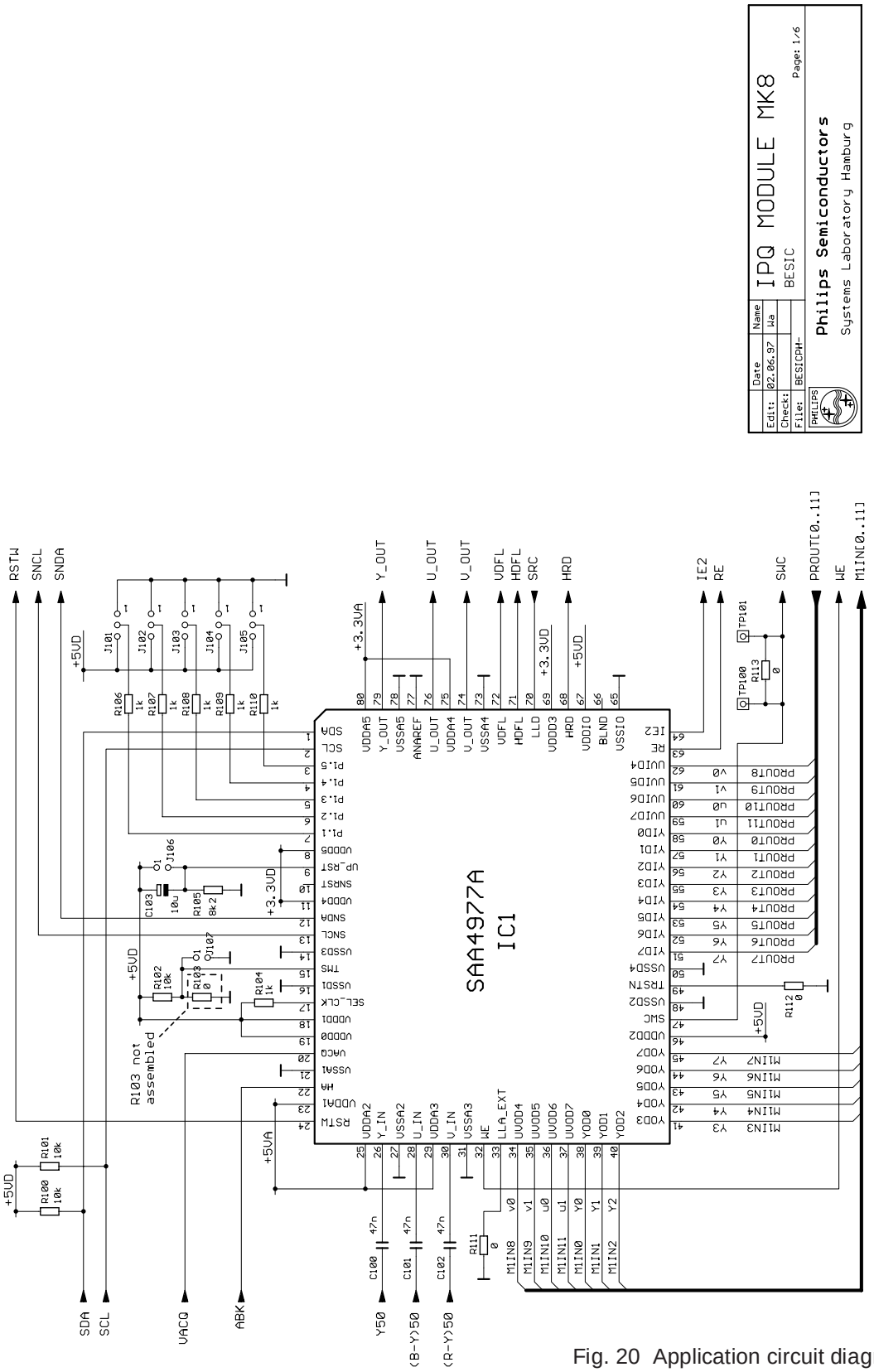

Fig. 20 Application circuit diagram, sheet 1

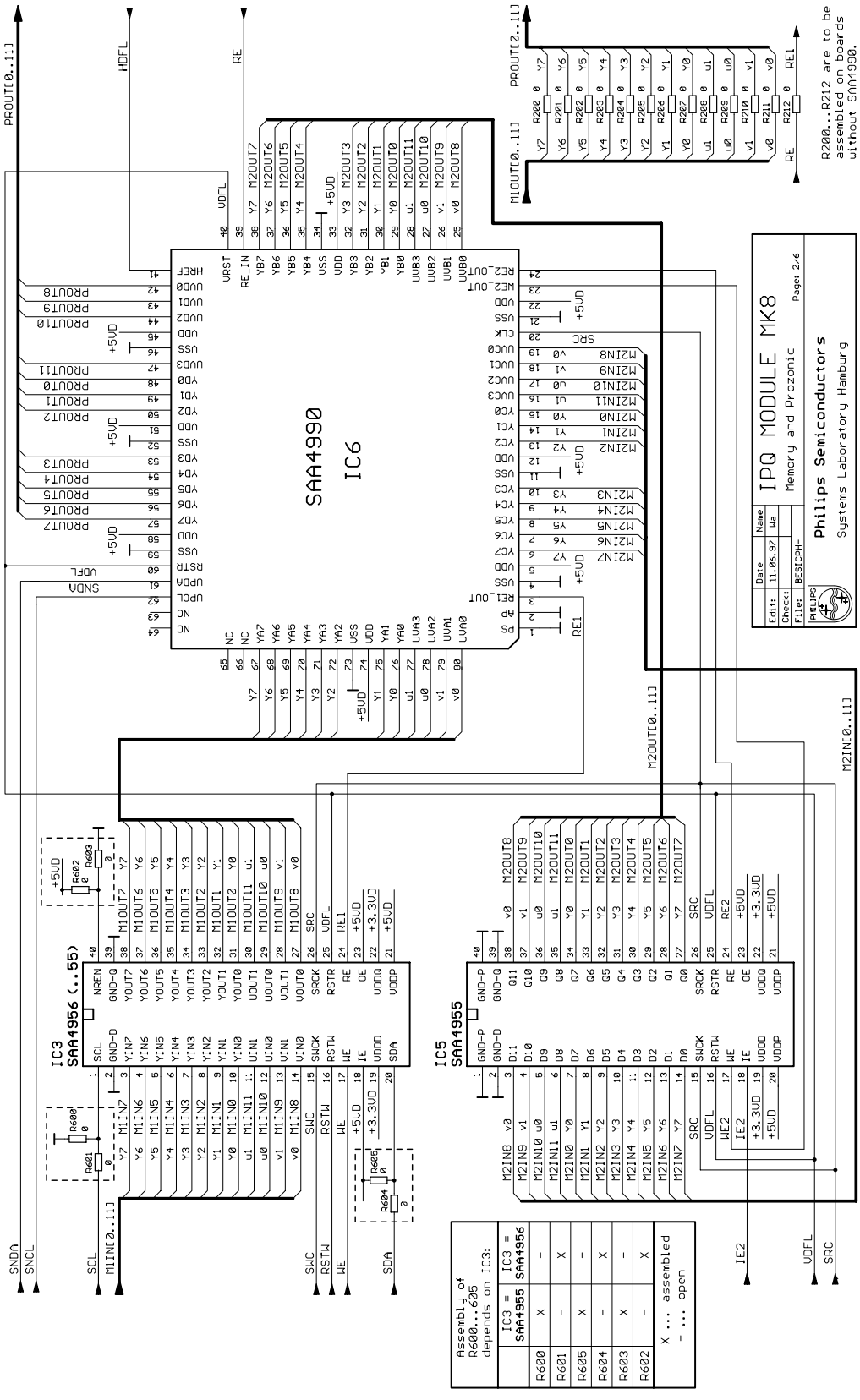

Fig. 21
Application circuit diagram, sheet 2

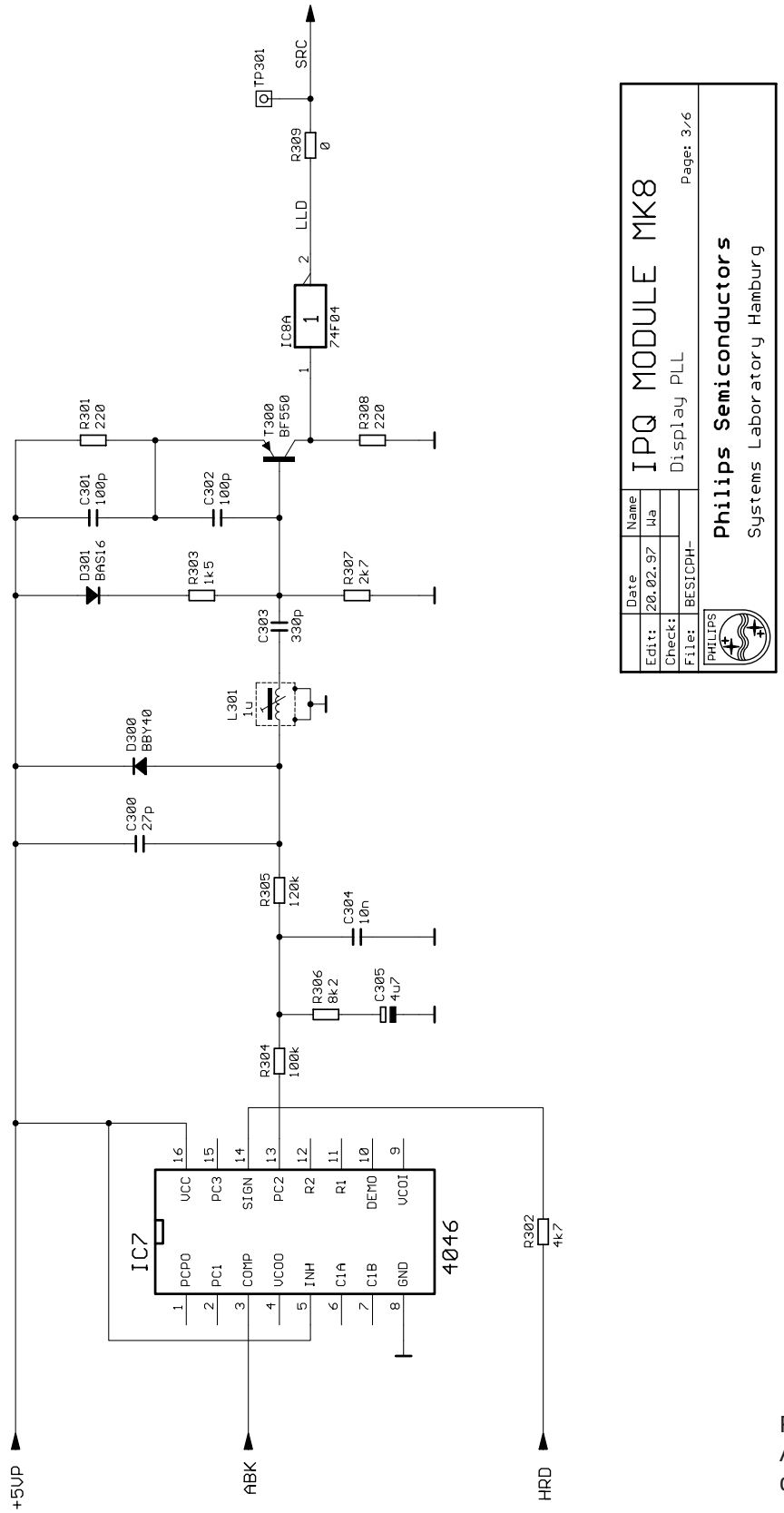

Fig. 22
Application circuit diagram, sheet 3

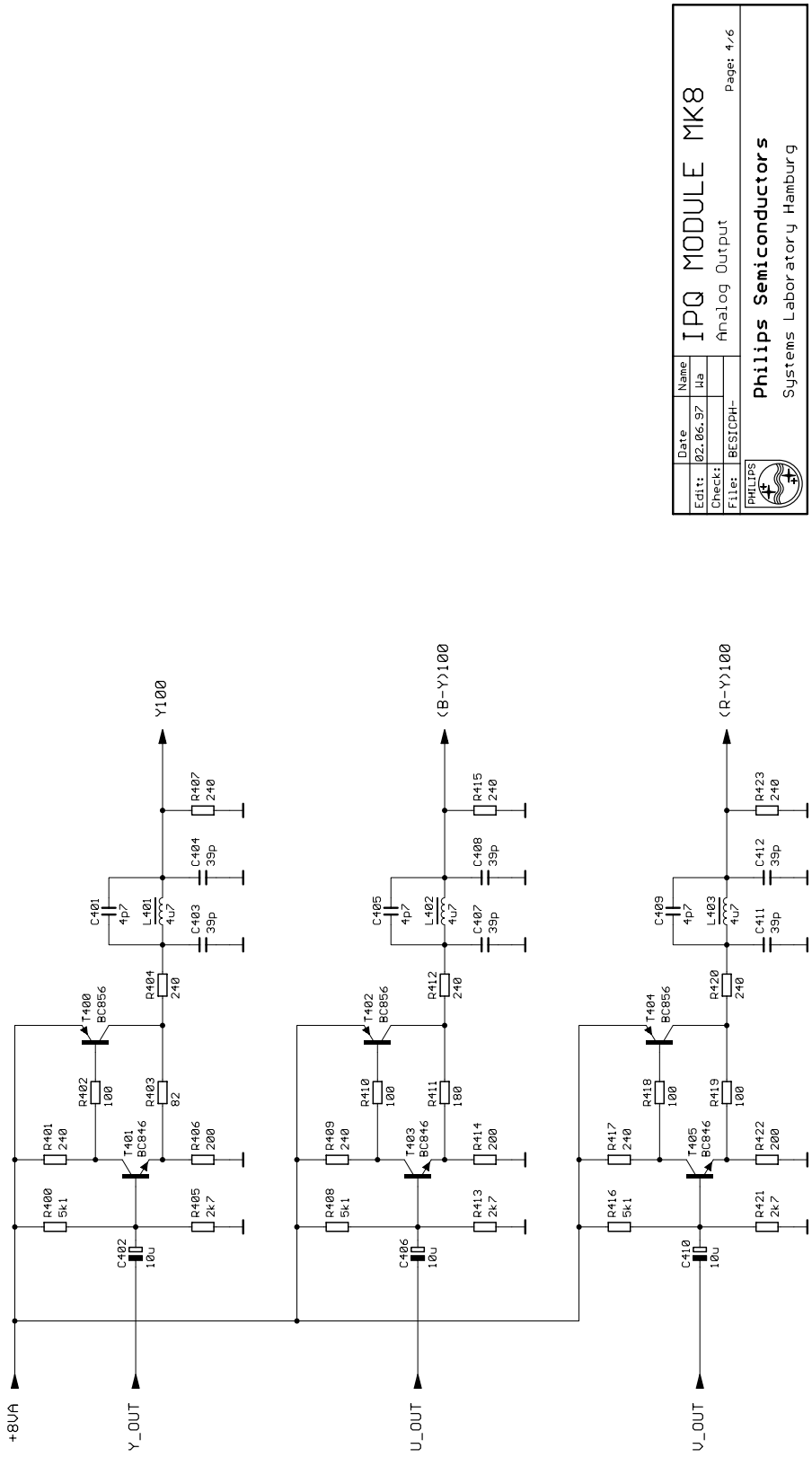

Fig. 23
Application circuit diagram, sheet 4

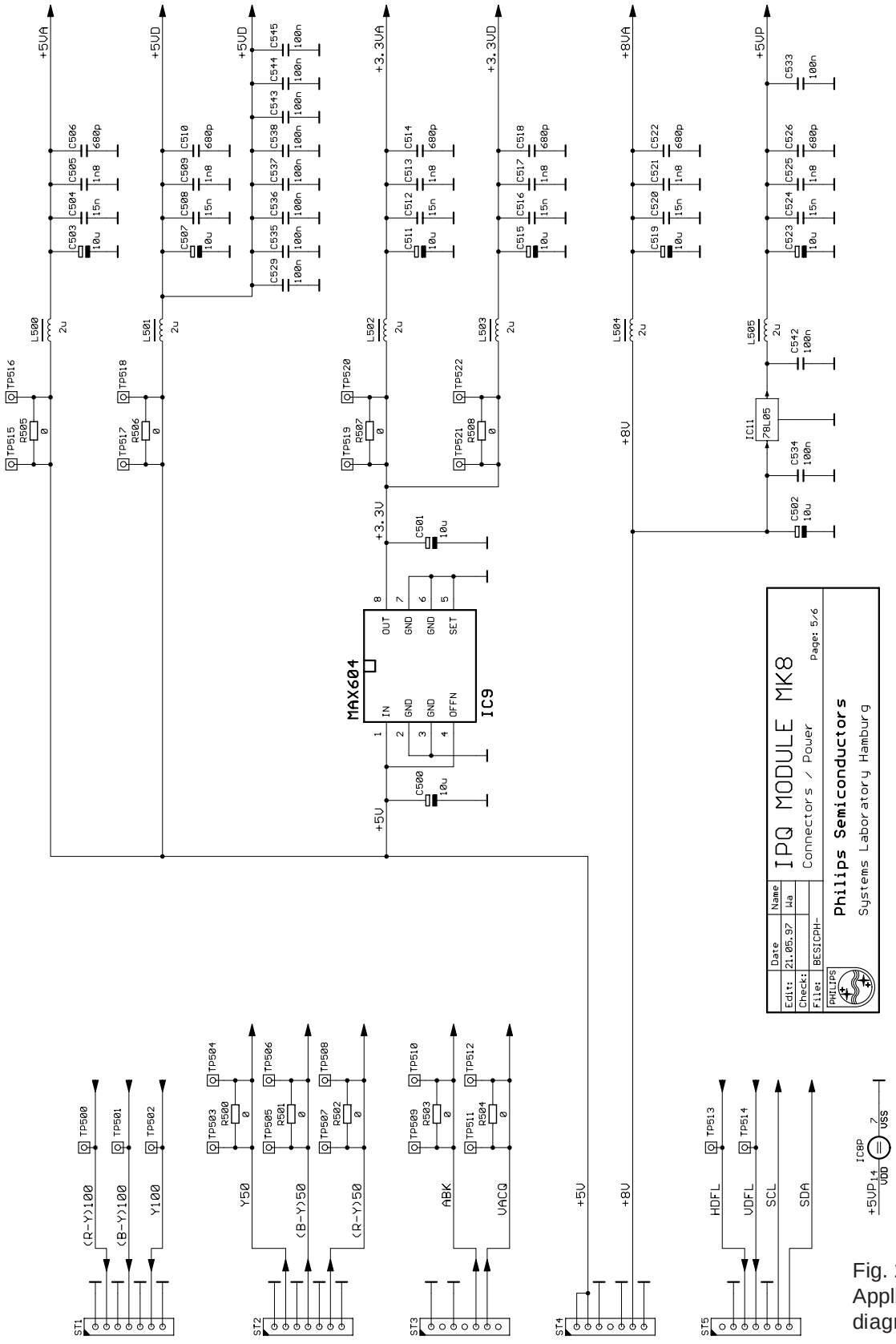

Fig. 24
Application circuit diagram, sheet 5

The 4-layer board measures 120 mm by 94 mm, the layout of each layer is given in fig. 17 to fig. 20, fig 21 shows the assembly plan of the board. The board is provided with additional footprints for TMS4C2972 memories.

6. References

[1] Lahann, Nils: I^2C-bus register specification for BESIC, Philips Semiconductors User Manual UM9701, 1997

[2] Waterholter, Heinrich: The SNERT bus specification, Philips Semiconductors Application Note AN95127, 1996

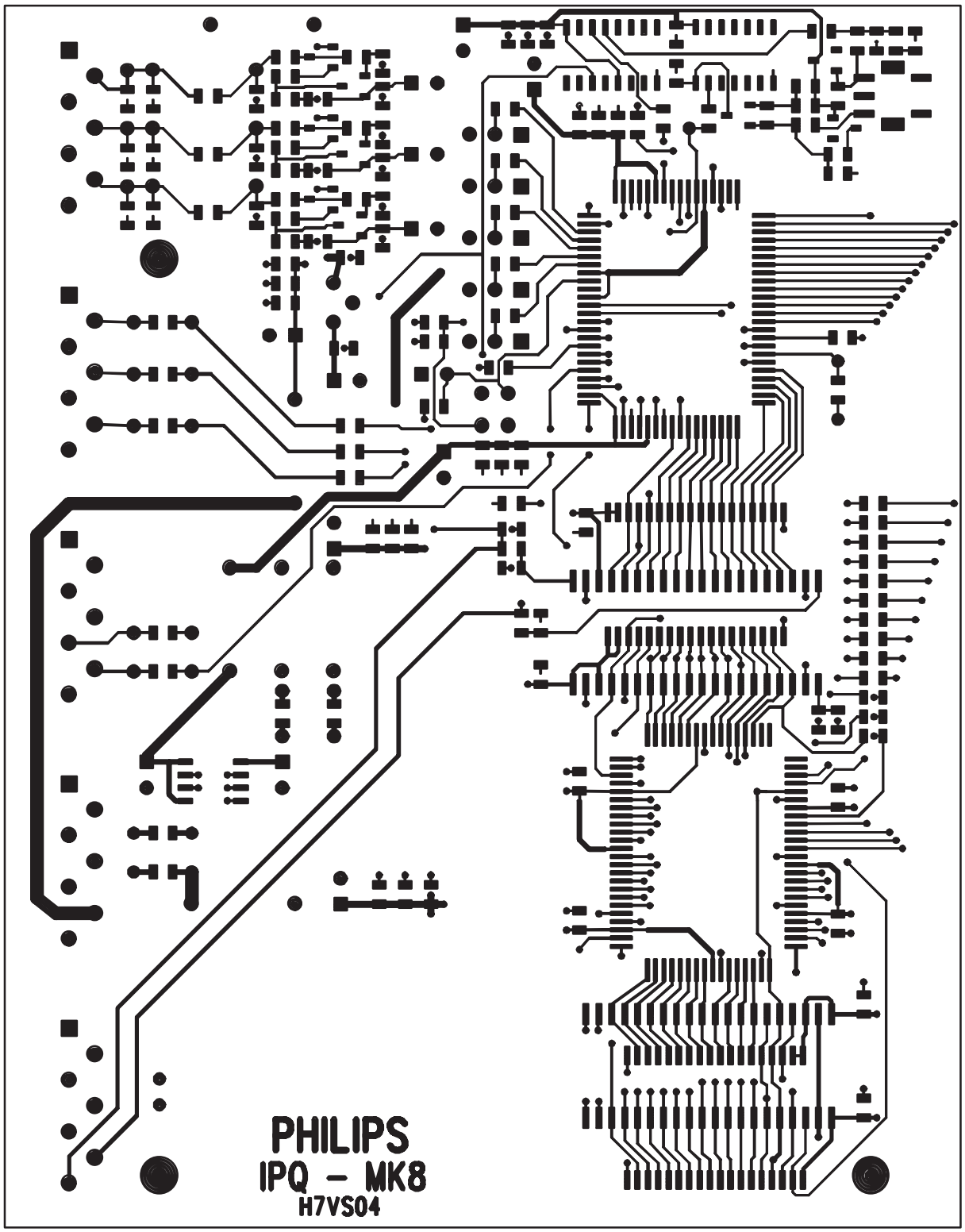

Fig. 25 PC board layout, layer 1 (top)

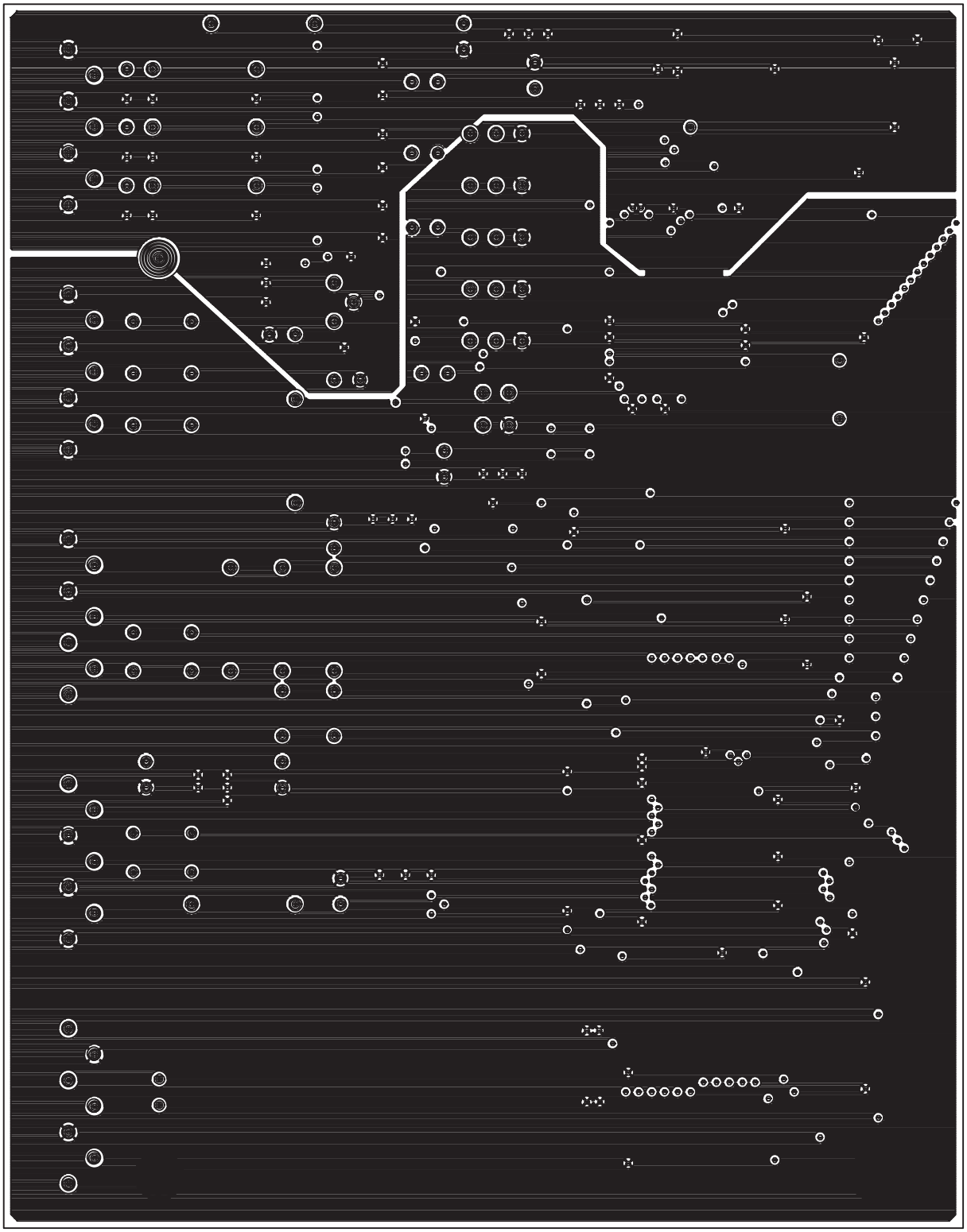

Fig. 26 PC board layout, layer 2

Fig. 27 PC board layout, layer 3

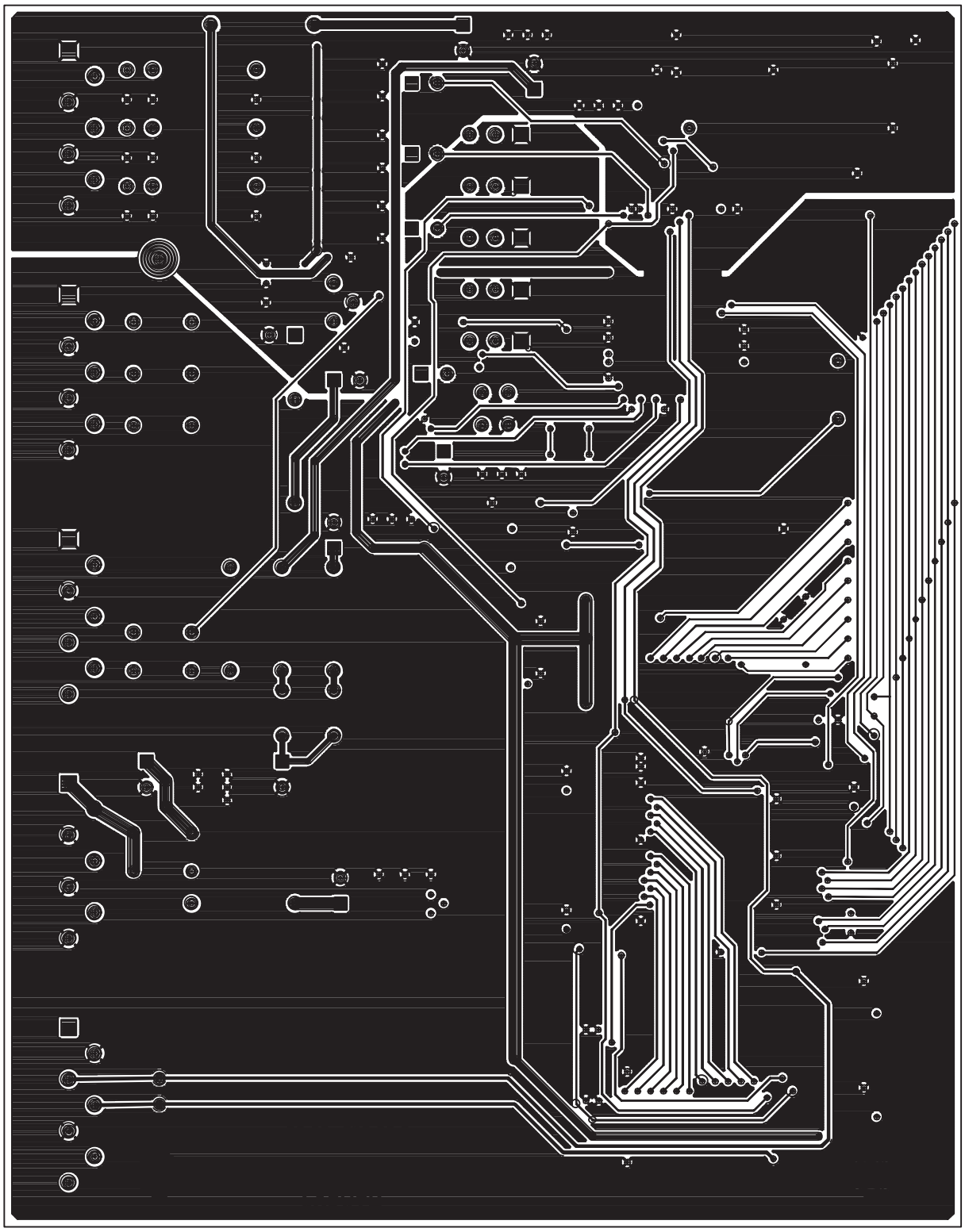

Fig. 28 PC board layout, layer 4 (bottom)

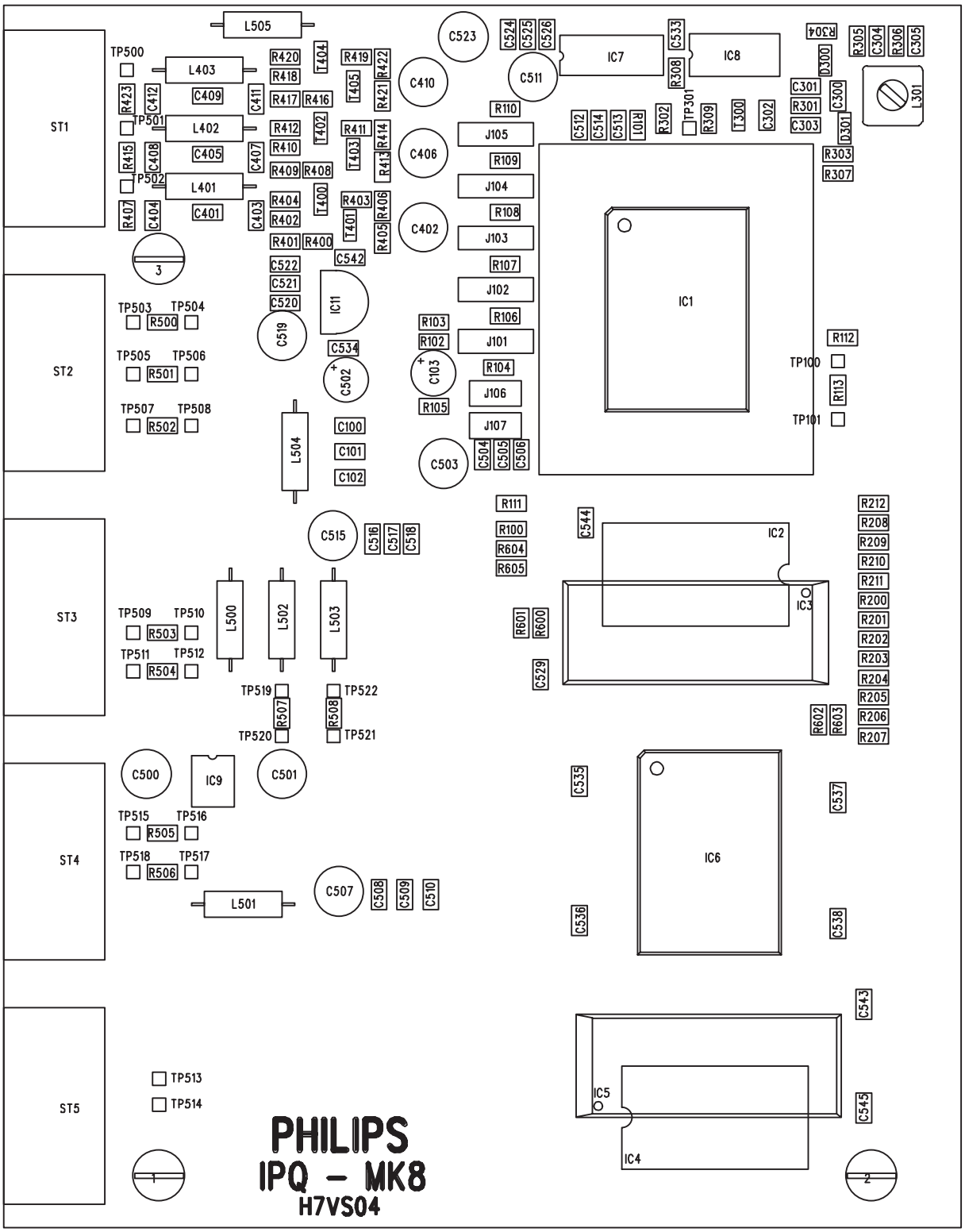

Fig. 29 PC board layout: assembly plan